C. REMARKS

Status of the Claims

Claims 1-8, 11, 13, 15-18, 20, and 22-29 are currently present in the Application, and claims 1, 11, 18, and 25 are independent claims. Claims 1, 8, 11, 13, 18, 20, and 25 have been amended, claims 9, 10, 12, 14, 19, and 21 have been cancelled, and no claims have been added.

Examiner Interview

Applicants note with appreciation the telephonic interview conducted between Applicants' representative, the Examiner, and the Examiner's trainer on March 7, 2006. During the telephonic interview, the Examiner and Applicants' representative discussed the 102 references (McCrory, Int. Pub. WO 98/19238 and Parrish et. al, U.S. Pat. No. 5,117,350). In particular, Applicants' representative discussed that Applicants' invention resides on a silicon substrate (a single device) and includes an on chip coherent multiprocessor bus. Applicants' representative continued to discuss that both McCrory and Parrish are "system" level disclosures that include off-the-shelf processors and printed circuit cards. Therefore, neither McCrory nor Parrish disclose Applicants' "single substrate" limitation or "on chip coherent multiprocessor bus" limitation.

In addition, Applicants' representative discussed that Parrish's "second processor" only has a private memory area, and does not include a non-private memory area as suggested by the Office Action. Applicants' representative suggested amending Applicants' independent claims to include particular limitations found in their respective dependent claims in order for Applicants' independent claims to read over the art of record. No agreement was reached regarding the claims.

Drawings

Applicants note that the Examiner did not indicate whether the formal drawings, filed with Applicants' application, are accepted by the Examiner. Applicants respectfully request that the Examiner indicate whether the formal drawings are accepted in the next office communication.

Claim Rejections

Claims 1-5, and 9-10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by McCrory (International Publication WO 98/19238, hereinafter "McCrory"). Applicants respectfully traverse these rejections. Applicants have amended claim 1 to include the limitations of claims 9 and 10. As such, claims 9 and 10 have been canceled in this response and, therefore, the rejections to these claims are moot. In addition, Applicants have amended claim 1 to include the term "silicon" substrate, which is supported in the specification and, therefore, no new matter is added.

Applicants claim 1 as amended is directed to a memory shared by a plurality of heterogeneous processors with limitations comprising:

- the shared memory;
- wherein the shared memory is accessible by one or more first processors that are adapted to process a first instruction set;
- wherein the shared memory is accessible by one or more second processors that are adapted to process a second instruction set; and
- wherein the shared memory, the first processors, and the second processors are included on one silicon substrate and are connected using an on chip coherent multi-processor bus.

Applicants' invention includes a shared memory, a first processor, one or more second processors, and an on chip coherent multi-processor bus, which are all included on a single **silicon substrate** (e.g., a single device). In contrast, McCrory discloses a "platform" that consists of **printed circuit cards.** Each printed circuit card includes individual, off-the-shelf processors (e.g., Intel 80486 and Intel Pentium) with standard Input/Output pins (page 12, lines 1-36). In fact, McCrory states that:

> "In a preferred HSMP system, one or more processors from a **first processor family are packaged on a single printed circuit card** along with necessary bus interface converters for coupling the card to a common bus. **Additional circuit cards include processors from other families of processors.** These circuit cards are coupled to the common bus through additional bus interface converters. The bus provides each processor with access to common IO devices and memory." (page 4, lines 5-13, emphasis added)

As can be seen from the above excerpt, McCrory packages one type of processor on one printed circuit card, and packages a different type of processor on an entirely different printed circuit card. McCrory then discloses using bus interface converters on each printed circuit card, which provides physical and logical external conversions for coupling the processors on the printed circuit cards to implementation specific communication mechanisms. McCrory never discloses combining a first processor type and a second processor type on the same printed circuit card. Therefore, McCrory never discloses including a first processor type, a second processor type, and shared memory on **one silicon substrate** as claimed by Applicants.

In addition, since McCrory discloses different processor types on different printed circuit cards, McCrory never teaches

or suggests an **on chip** coherent multi-processor bus that couples the first processor, the second processor, and the shared memory as claimed by Applicants. Therefore, since McCrory does not teach or suggest all the limitations of claim 1 as amended, amended claim 1 is allowable over McCrory. Each of the remaining claims 2-5 each depended, either directly or indirectly, upon allowable independent claim 1. Therefore, claims 2-5 are allowable for at least the same reasons as amended claim 1 is allowable.

Claims 11-13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Parrish et. al, (U.S. Patent No. 5,117,350, hereinafter "Parrish"). Since claims 17-20 and 24-29 are discussed in the same section as claims 11-13 in the Office Action, Applicants assume that claims 17-20 and 24-29 are also rejected under 35 U.S.C. § 102(b) as being anticipated by Parrish. Applicants respectfully traverse these rejections.

Claims 8, 14, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCrory in view of Brown (NPL Document "The Design of ARMphetamin 2," hereinafter "Brown"). Since the independent claims of claims 14 and 21, which are claims 11 and 18 respectively, were rejected using Parrish, Applicants assume that claims 14 and 21 are actually rejected under 35 U.S.C. § 103(a) as being unpatentable over **Parrish** in view of Brown. Applicants respectfully traverse these rejections.

Applicants have amended independent claims 11 and 18 to include the limitations of dependent claims 12, 14, 19, and 21 into their respective independent claims. As such, Applicants have canceled claims 12, 14, 19, and 21 in this response and, therefore, rejections to these claims are moot.

As amended, independent claims 11 and 18 are directed to sharing memory between a plurality of heterogeneous processors with limitations comprising:

- allocating a first memory partition on the shared memory that corresponds to the memory request, the first memory partition accessible by one or more first processors that are adapted to process a first instruction set;
- assigning a second memory partition on the shared memory to one or more second processors that are adapted to process a second instruction set;
- managing the first memory partition and the second memory partition using a common memory map; and
- wherein the common memory map includes a plurality of regions, wherein at least one of the regions is selected from the group consisting of an external system memory region, a local storage aliases region, a TLB region, an MFC region, an operating system region, and an I/O devices region.

Applicants' invention uses a common memory map to share memory between a plurality of heterogeneous processors. The common memory map includes common effective addresses, common virtual addresses, and common physical addresses. As such, the common memory includes a plurality of regions, all accessible by each of the plurality of heterogeneous processors. The Office Action uses Brown to reject Applicants' "plurality of regions" limitations. However, after closer review, Brown does not teach a common memory map that includes a plurality of regions that are used by **both** a first processor type and a second processor type as claimed by Applicants. The reason being is that Brown's memory mapping system applies to a **single** processor type system. Furthermore, Parrish discloses that:

> "The memory in the system address space is addressable by system physical addresses for memory in each node. The node physical addresses are translatable to and from the system physical addresses by partitioning maps located in **partition tables <u>at each node</u>**." (Abstract, emphasis added)

As can be seen from the above excerpt of Parrish, Parrish teaches memory partition tables specific to each node (processor), and never teaches a common partition table that is used by both a first processor type and a second processor type that are located in different nodes. Therefore, the combination of Parrish with Brown does not result in a common memory map that includes a plurality of regions that are used by **both** a first processor type and a second processor type as claimed by Applicants.

Therefore, since neither Parrish nor Brown teach or suggest, either in whole or in combination with each other, all the limitations of claim 11 as amended, amended claim 11 is allowable over Parrish in view of Brown. Claim 18 is a computer program product claim including the same limitations of claim 11 and, therefore, is allowable for the same reasons as claim 11 is allowable.

Notwithstanding the fact that claim 8 is dependent upon claim 1 and, therefore, allowable for the same reasons as claim 1 is allowable, claim 8 includes the "plurality of regions" limitation that is not taught or suggested by Brown (discussed above). In addition, when combining Brown with McCrory, the result is a system that still includes a printed circuit board for each type of processor, whereby Brown's memory mapping system runs on each printed circuit board for **a single processor type**. For example, if McCrory uses processor type A on card A and processor type B on card B, the combination of McCrory with

Brown results in processor type A on card A using memory map A and processor type B on card B using memory map B. This is different than using a **common memory map** that includes a plurality of regions that are used by **both** processor type A and processor type B as claimed by Applicants. Therefore, since neither McCrory nor Brown teach or suggest, either in whole or in combination with each other, all the limitations of claim 8, claim 8 is allowable over McCrory in view of Brown.

Independent claim 25 is directed to a memory shared by a plurality of heterogeneous processors with limitations comprising:

- the memory, wherein the memory includes one or more non-private storage areas, the non-private storage areas **included in one or more second processors** that are adapted to process a second instruction set and access the memory; and
- wherein the shared memory is accessible by one or more first processors that are adapted to process a first instruction set and access the memory.

Applicants claim that non-private storage areas are **included in** one or more second processors. During the Examiner interview, the Examiner discussed that Parrish's Figure 2 shows both a private memory and a non-private memory. After closer review, however, Parrish's Figure 2 shows Industry Standard Computer (ISC) 113 including only private memory (IPM), and the non-private memory is **external** to ISC 113, which is not the same as claimed by Applicants. Furthermore, Applicants' claim that the local memory is included in a **second processor**, and not an **entire computer system** as disclosed by Parrish. Therefore, since Parrish does not teach or suggest all the limitations included in claim 25, claim 25 is allowable over Parrish.

Each of the remaining claims 12-13, 17, 19-20, 24, and 26-29 depend, either directly or indirectly, upon one of the allowable independent claims 11, 18 and 25 discussed above. Therefore, claims 12-13, 17, 19-20, 24, and 26-29 are also allowable for at least the same reasons as their independent claims are allowable.

Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCrory in view of Parrish. Applicants respectfully traverse these rejections.

Claim 6 depends upon claim 4, which results in limitations of:

- wherein each second processor further comprises:
  - a synergistic processing unit;
  - a local storage;
  - a memory management unit, the memory management unit including a direct memory access controller; and
  - wherein the local storage is divided into a private storage and a non-private storage.

The Office Action uses Parrish to reject Applicants' limitation of a second processor **including** a local storage area that is divided into a private storage and a non-private storage. As discussed above, Parrish never teaches or suggests a second processor including a private storage **and a non-private storage.** The Office Action does not suggest that McCrory teaches or suggests such limitation, and indeed McCrory does not. Therefore, since neither McCrory nor Parrish teach or suggest, either in whole or in combination with each other, all the limitations included in claim 6, claim 6 is allowable over McCrory in view of Parrish. Claim 7 is dependent upon claim 6

and, therefore, is allowable for at least the same reasons as claim 6 is allowable.

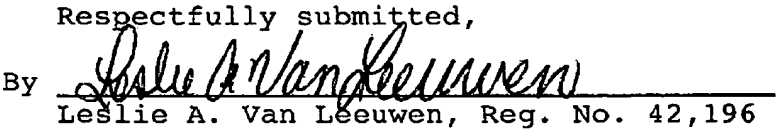
Claim 13, 15, 16, 22, and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Parrish in view of McCrory. Applicants respectfully traverse these rejections. Each of claims 13, 15, 16, 22, and 23 depend, either directly or indirectly, upon one of the allowable independent claims 11 and 18. Therefore, claims 13, 15, 16, 22, and 23 are also allowable for at least the same reasons as their independent claims are allowable.

Conclusion

As a result of the foregoing, it is asserted by Applicants that the remaining claims in the Application are in condition for allowance, and Applicants respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner contact the Applicants' attorney listed below if the Examiner believes that such a discussion would be helpful in resolving any remaining questions or issues related to this Application.

Respectfully submitted,

By 

Leslie A. Van Leeuwen, Reg. No. 42,196
Van Leeuwen & Van Leeuwen
Attorney for Applicants
Telephone: (512) 301-6738
Facsimile: (512) 301-6742

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☒ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.